REMARKS

Claims remaining in the present application are Claims 16-36. Claims 1-15 have been cancelled, without prejudice. Claim 16 has been amended. Claims 21-36 have been added. No new matter has been added as a result of these claim amendments.

SPECIFICATION

The rejection asserts that the specification fails to provide U.S. Application Serials in several places. Applicants respectfully direct the Examiner's attention to the previously submitted preliminary amendment, which provided these application numbers. Applicants have attached a copy of the previously filed preliminary amendment hereto.

CLAIM REJECTIONS

35 U.S.C. § 112, ¶1, enablement

Claims 1, 9, and 16 are rejected under 35 U.S.C. § 112, ¶1, enablement. Claims 1 and 9 have been cancelled, without prejudice. Therefore, the rejection to Claims 1 and 9 is moot. The rejection to Claim 16 is respectfully traversed for the following reasons.

Applicants respectfully assert that Claim 16 is fully enabled by the specification. The rejection asserts that the Specification does not refer to, or

describe the elements in Claim 16 of, "allowable position overlaying at least one of said resource images." Applicants respectfully disagree.

Applicants respectfully assert that the Specification is not required to use the exact same terms and phrases as the claims to enable the claims. The Specification clearly enables the claim element in question. For example, the Specification at page 14, lines 1-3, as amended by the preliminary amendment discloses, "[r]eferring now to step 250 of Figure 2, the user may then select the new position by clicking on the select position button 372 when the user module 304 is *on* the desired programmable system block or blocks 410. Furthermore, the Specification at page 15, lines 20, as amended by the preliminary amendment discloses, "[w]hen the user module 304 is placed (e.g., instantiated) on a particular programmable system block 410 the register settings and parameter settings are mapped to a physical register address on the chip."

Applicants further respectfully assert that the drawings may be used to support the enablement requirement. Applicants refer to Figure 1B, Figure 1C, Figure 3A, Figure 3B, Figure 3C, Figure 4, Figure 5A, Figure 5B, Figure 5C, Figure 6A, Figure 6B, Figure 6C, and Figure 6D, which depict various allowable positions (for respective user module) overlaying at least one resource image in a graphical user interface.

For example, Figure 1B depicts six user modules selected for placement (ADCINC12_1, Counter16_1, DAC8_1, INSAMP_1, INSAMP_2, PWM16_1, and UART_1). The resource images include DBA00, DBA01, DBA02, DBA03, DCA04, DCA00, DBA05, DCA06, DCA07 (partially visable), ACA00, ACA01, ACA02, ACA03, ASA10, ASB11, ASA12, ASB13. Applicants also refer to the Specification at page 9, lines 3-24, which refers to the user modules and resource images in Figure 1B. Referring to Figure 1B, user modules are overlaying resource images. For example, ADCINC12_1 overlays resource images DBA00 and DBA01. Thus, the specification, including the drawings, fully enables the claim element of, "an allowable position [of a module] overlaying at least one of said resource images."

Applicants also respectfully assert that the rejection's position that Greidinger (U.S. Patent No. 6,449,761) teaches this element is inconsistent with an assertion that the present application fails to enable this element. That is, a patent application is not required to describe details that are known in the art. Thus, the rejection's assertion that the prior art teaches the element is inconsistent with an assertion that the present application does not enable this element. However, as discussed below, Applicants assert that Greidinger does not teach this element.

35 U.S.C. § 112, ¶2

Claims 1, 9, and 16 are rejected under 35 U.S.C. §112, ¶2. Claims 1 and 9 have been cancelled, without prejudice. Therefore, the rejection to Claims 1 and 9 is moot. The rejection to Claim 16 is respectfully traversed for the following reasons.

The rejection asserts that there is insufficient antecedent basis for certain limitations in the claims. With respect to Claim 16, the rejection asserts that the limitation "allowable position overlaying at least one of said resource images," lacks sufficient antecedent basis. Applicants respectfully assert that the limitation in question is recited as "an allowable position overlaying at least one of said resource images." Therefore, the only possible antecedent basis issue in the claims would be the element said resource images, which finds clear antecedent basis in Claim 16.

With respect to antecedent basis in the specification for the limitations, "allowable position overlaying at least one of said resource images," Applicants note that the mere fact that a term or phrase used in a claim does not have an exact antecedent in the specification does not mean that the claim is indefinite under 35 U.S.C. §112, ¶2. Applicants are given a great deal of latitude as to how they choose to define their invention, so long as the terms and phrases define the invention with a reasonable degree of clarity and precision (see e.g., MPEP 2173.05(e)). For at least the reasons

discussed in the response to the 35 U.S.C. §112, ¶1 rejection, the terms in the phrase "an allowable position overlaying at least one of said resource images" define the invention with a reasonable degree of clarity and precision.

For the forgoing reasons, Claim 16 complies with 35 U.S.C. §112, ¶2.

35 U.S.C. 102(e)

Claims 1-6 and 8-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Greidinger et al. U.S. Patent No. 6,449,761 (hereinafter, Greidinger). Claims 1-15 have been cancelled, without prejudice. Therefore, the rejection to Claims 1-6 and 8-15 is moot. The rejection to Claims 16-19 is respectfully traversed for the following reasons.

Independent Claim 16 recites, in part:

> b) said user placing said first module in a graphical user interface, wherein said graphical user interface comprises a plurality of resource images representing a layout of resources in said programmable device in which to implement said modules, and wherein and said placement is an allowable position overlaying at least one of said resource images and is based on characteristics of said first module and characteristics of said resources.

Applicants respectfully assert that Greidinger fails to teach or suggest these claimed limitations. Greidinger does not teach or suggest a graphical user

interface comprising resource images representing a layout of resources in a programmable device in which to implement modules, as claimed. Nor does Greidinger teach or suggest placement (of a module) overlaying at least one of said resource images, as claimed.

Greidinger may teach a graphical user interface (GUI) in which "cells" are placed. Figure 3 of Greidinger shows a GUI that depicts cell/sub-cells (e.g., components/subcomponents) placed with chip boundaries drawn around the cells (e.g., initial layout boundary 310A and a final layout boundary). The cells do not represent resources in a programmable device in which to implement said modules, but rather user desired functions to incorporate into the design. The fact that the cells can be re-arraigned by moving cells, replacing one cell for another with a different geometry, or even replacing one cell with a cell with different features (col. 6, lines 3-28), clearly indicates that the cells do not represent a layout of resources in a programmable device in which to implement modules, as claimed.

Next, Greidinger does not teach that the placement (of the module) overlays at least one resource image. As Greidinger fails to show the claimed resource images, Greidinger cannot teach the overlaying at least one resource image.

Further, with respect to Figure 3, Applicants understand Greidinger to teach a sub-cell within a cell (e.g., 328A, 326A). However, as previously discussed the cells are not a resource in a programmable device. Rather, the cells represent functions that a user wishes to incorporate into a chip design.

Referring to Figure 6, Greidinger depicts cells 628 and 630 being aligned with one another. However, neither cell overlays a resource image. Figure 6 also shows a "keep-in" restraint that keeps cell 324A within a boundary. However, neither the small boundary 636 nor the large boundary 310A constitute resources in which to implement modules. That is, the boundaries do not define resources in which to implement modules.

For the foregoing reasons, Greidinger fails to teach or suggest the limitations of Claim 16.

Claims 17-19 depend from Claim 16, which is believed to be allowable for the foregoing reasons. As such, it is respectfully submitted that Claims 17-19 are not anticipated by Greidinger.

35 U.S.C. 103(a)

Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greidinger in view of Bjorksten et al. U.S. Patent No. 5,930,148 (hereinafter, Bjorksten). Claim 7 has been cancelled, without

prejudice. Therefore, the rejection is moot. The rejection to Claim 20 is respectfully traversed for the following reasons.

Claim 20 depends from Claim 16, thus incorporating limitations discussed in the response to Claim 16. For reasons discussed in the response to Claim 16, Greidinger fails to teach or suggest the limitations discussed above. Bjorksten fails to remedy this deficiency in that *the combination* fails to teach these limitations. Therefore, neither Greidinger nor Bjorksten, alone or in combination, teach or suggest limitations of Claim 20.

NEW CLAIMS

New Claim 21 recites, in part:

> requesting a valid placement for said module in a graphical user interface comprising resource images defining programmable resources in said programmable device, said valid placement specifying at least one of said resource images.

Applicants respectfully assert that the cited art fails to teach or suggest these limitations. For example, the cited art does not teach or suggest requesting a valid placement for a module in a graphical user interface comprising resource images defining programmable resources in said programmable device.

New Claim 30 recites, in part:

requesting valid placements for said module in said graphical user interface, each of said valid placements specifying at least one of said resource images;

receiving respective indications of valid placements for said module in said graphical user interface.

Applicants respectfully assert that the cited art fails to teach or suggest these limitations. For example, the cited art does not teach or suggest requesting valid placements for said module in said graphical user interface, each of said valid placements specifying at least one of said resource images. Further, the cited art does not teach or suggest receiving respective indications of valid placements for said module in said graphical user interface.

Claims 22-29 and 31-36 depend from Claims 21 and 30. Therefore, Claims 22-29 and 31-36 are respectfully believed to be allowable.

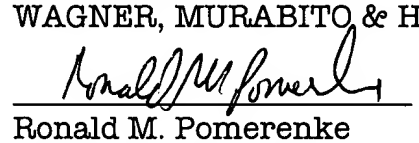
CONCLUSION

Should the Examiner have a question regarding the instant response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Based on the arguments and amendments presented above, it is respectfully submitted that Claims 16-36 overcome the rejections and objections of record and, therefore, allowance of Claims 16-36 is earnestly solicited.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: 4/19, 2005



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CYPR-CD01168M

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

Manfred BARTZ et al. : GROUP ART UNIT:

SERIAL NO: 09/989,571 :

FILED: NOVEMBER 19, 2001 : EXAMINER:

FOR: METHOD FOR DESIGNING A CIRCUIT FOR PROGRAMMABLE MICROCONTROLLERS

PRELIMINARY AMENDMENT

COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to examination of the above-identified application, consideration of the following Amendments and Remarks is respectfully requested.

IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 4 with the following new paragraph:

The present invention relates to the field of programmable single-chip systems. Specifically, the present invention relates to a method for designing a circuit to be implemented in a target device, such as a microcontroller, using a graphical software program.

Please replace the paragraph beginning at page 4, line 10 with the following new paragraph:

A method to facilitate circuit design using a software program with a graphical user interface is disclosed. First a user selects a module from a catalog of available modules. The module may be for implementing an amplifier, timer, pulse width modulator, etc. This causes information related to the selected module to be displayed. For example, a schematic and data sheet for the selected

module may be displayed. Next, the user requests a position and places the selected module in a graphical user interface, which represents the resources available to implement the available modules. For example, the resources may be programmable system blocks. Additional user modules may then be selected and placed.

Please replace the paragraph beginning at page 4, line 21 with the following new paragraph:

The user then configures the circuit by selecting circuit parameters for the user modules (e.g., amplifier gain), pin configurations, and interconnections between programmable system blocks. The user may then edit source code used to cause the user modules to perform their functions.

Please replace the paragraph beginning at page 5, line 1 with the following new paragraph:

Another embodiment allows the user to select a new position (e.g., new programmable system block or blocks) for a selected user module. In response to such a user request, a new potential position is computed and displayed for the user module.

Please replace the paragraph beginning at page 7, line 6 with the following new paragraph:

Figure 6A, Figure 6B, Figure 6C, and Figure 6D are illustrations of graphical user interfaces for configuring interconnections between programmable system blocks, according to an embodiment of the present invention.

Please replace the paragraph beginning at page 9, line 2 with the following new paragraph:

Referring now to Figure 1B, a user module placement work-space includes a resource graphic window 360 illustrating the placement of user modules 304 with respect to the available resources (e.g., available programmable system blocks 410 of a microcontroller) in a hardware layout graphical display. Throughout this application the term resource image may denote the blocks 410 upon which

user modules 304 are placed in window 360. As the resource images may represent programmable system blocks in one embodiment, the resource images may be referred to as programmable system blocks for convenience. It will be understood that the resource images may represent other resources however, as the present invention is not limited to implementing the user modules 304 in programmable system blocks. Figure 1B shows a number of digital programmable system blocks 410a along the top row (e.g., the blocks labeled DBA00, DBA01, etc.), as well as four columns of analog programmable system blocks 410b (e.g., the blocks labeled ACA00, ACA01, etc.). The present invention is well suited to using any number of analog and digital programmable system blocks 410. Furthermore, the blocks in graphic window 360 are not limited to representing programmable system blocks.

Please replace the paragraph beginning at page 9, line 19 with the following new paragraph:

A single user module 304 may map to one or more programmable system blocks 410. Color coding (not shown) may be used to relate the user modules 304 of selected modules window 306 with their schematic placement in resource graphic window 360. The analog 410b and digital 410a programmable system blocks may be more generally defined as two different classes to which a user module 304 maps. The present invention is well-suited to having many different classes.

Please replace the paragraph beginning at page 10, line 2 with the following new paragraph:

Referring now to Figure 1C, a pin-out configuration work-space is shown. The pin-out configuration work-space allows the user to connect programmable system blocks 410 to input/output (I/O) pins, as well as configure the I/O pins' drive characteristics. In one embodiment, a pin configuration window 380 may be used to configure pins. Pin configuration window 380 has a port column 381, a select column 382, and a drive column 383. In another embodiment, a user

may set pin configurations by clicking on the GUI of the chip 610. The operation of these features will be discussed more fully herein.

Please replace the paragraph beginning at page 11, line 11 with the following new paragraph:

User modules 304 may require multiple programmable system blocks 410 to be implemented. In some cases, user modules 304 may require special ports or hardware which will limit the number of programmable system blocks 410 that can be used for their implementation. The process of mapping a user module 304 to programmable system blocks 410, such that the user module 304 is realized within the microcontroller, may be referred to as "user module placement." An embodiment automatically determines the possible placements of a user module 304 based on an Extensible Markup Language (XML) user module description and the hardware description of the underlying chip. However, the present invention is not limited to using XML descriptions. The potential placement positions may be automatically inferred based on the XML input data. Therefore, the placement process of embodiments of the present invention is data driven.

Please replace the paragraph beginning at page 11, line 24 with the following new paragraph:

Referring to step 220 of Figure 2, a user then requests a possible placement for a user module 304 in the resource area 360. One or more programmable system blocks 410 may be highlighted to indicate a possible position for the user module 304 based on, for example, XML input data. For example, referring to Figure 1B, the ADCINC12_1 user module 304 has been selected for placement in the window 360. This user module 304 requires two digital blocks 410a and one analog block 410b. The digital programmable system blocks 410a labeled DBA00 and DBA01 are highlighted to indicate a possible position for the ADCINC12_1 user module 304. Referring now to Figure 3A, the analog programmable system block 410b labeled ASB20 is highlighted to indicate that it is a possible position for the analog portion of the ADCINC12_1 user module 304. Embodiments may

use color coding to associate the highlighting color with a unique color assigned to that user module 304.

Please replace the paragraph beginning at page 12, line 12 with the following new paragraph:

User module placement is described in co-pending U.S. patent application serial number 09/989,762, filed concurrently herewith, entitled "A SYSTEM AND METHOD FOR PERFORMING NEXT PLACEMENTS AND PRUNING OF DISALLOWED PLACEMENTS FOR PROGRAMMING AN INTEGRATED CIRCUIT," by Ogami et al., attorney docket number CYPR-CD01175M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 12, line 19 with the following new paragraph:

Referring now to Figures 3A-3C and to step 240 of Figure 2, after placing a user module 304, a user may desire to move it to another programmable system block 410 (or blocks). In step 240, the user may request a new position for the user module 304 by, for example, clicking a next placement icon 371. In response to this, a new placement may be computed and displayed. Figures 3A-3C illustrate three possible positions for the analog portion of the ADCINC12_1 user module 304. Placements that are incompatible with the user module requirements are automatically pruned out by the software and therefore are not displayed as valid placements. In one embodiment, all positions are shown to the user, sequentially, each time the next placement icon 371 is selected. However, if a potential placement involves a programmable system block 410 that has already been used (e.g., by another placed user module 304), then in these cases the place user module icon 372 is grayed out indicating that this placement is only valid if the resources were vacant. This allows the user to see all possible placements.

Please replace the paragraph beginning at page 14, line 1 with the following new paragraph:

Referring now to step 250 of Figure 2, the user may then select the new position by clicking on the select position button 372 when the user module 304 is on the desired programmable system block or blocks 410.

Please replace the paragraph beginning at page 14, line 5 with the following new paragraph:

User module next placement is described in co-pending US patent application serial number 09/989,781, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR DECOUPLING AND ITERATING RESOURCES ASSOCIATED WITH A MODULE," by Ogami et al., attorney docket number CYPR-CD01180M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 14, line 12 with the following new paragraph:

The user may repeat steps 210 through 250 to add more user modules 304. Each time a new user module is selected, a system resource window is updated. Referring again to Figure 1A, for each User Module 304 selected, the system updates the data in a resource manager window 350 with the number of occupied programmable system blocks 410, along with RAM and ROM usage used by the current set of "selected" User Modules 304. The system may also prevent a user from selecting a User Module 304 if it requires more resources than are currently available. Tracking the available space and memory of configurations for the design may be performed intermittently during the whole process of configuring the microcontroller. There is also a live graph tracking the programmable system blocks 410 used by percentage. The RAM and ROM monitors track the amount of RAM and ROM required to employ each selected User Module 304.

Please replace the paragraph beginning at page 15, line 1 with the following new paragraph:

After the user has selected one or more user modules 304, the user selects global parameters and user module parameters. Embodiments allow a user to select user module parameters, such as, for example, the gain of an amplifier, a clock speed, etc. Referring now to Figure 4 and to step 260 of Figure 2, in response to a user clicking on a region on a programmable system block 410 an interface 510 is displayed which allows the setting of user module parameters. For example, the user may place "the cursor" over the lower-left corner of a programmable system block 410 to set input parameters. The system may display a superficial chip or a changed cursor in response to this. The user may then left-click a mouse, for example, to bring up a user module parameter window 510 to configure the user module input parameters. The process may be repeated in the lower-right corner of the programmable system block 410 for output parameters and on the upper-left corner for clock parameters. The present invention is not limited to these steps for bringing up a user module pop-up window 510, however. The system may then display the selected parameters in a user module parameter window 520. Various pop-up windows may be data driven in that the contents of the pop-up window may depend on, for example, the user module 304 selected. Alternatively, user parameters may be set in the user module parameter window 520.

Please replace the paragraph beginning at page 15, line 20 with the following new paragraph:

When the user module 304 is placed (e.g., instantiated) on a particular programmable system block 410 the register settings and parameter settings are mapped to a physical register address on the chip. This also associates interrupt vectors that the user module 304 uses based on the programmable system block 410. Each of the digital blocks 410a maps to one vector and each column of analog blocks 410b maps to another vector. Once the user modules 304 are placed and the parameters are set, all the physical address registers that are associated with that user module 304 are fixed and the register values are determined.

Please replace the paragraph beginning at page 16, line 12 with the following new paragraph:

Referring now to Figures 5A-5C and to step 270 of Figure 2, the user selects input/output pin configurations. One embodiment provides for a graphical user interface for facilitating the configuration of I/O pins in a microcontroller software design tool. By specifying a programmable system block 410 to a pin-out, a user may make a physical connection between the software configuration and the hardware (e.g., the microcontroller). Each pin has a pin number associated therewith. Referring to Figure 5A, when the user clicks on a pin of GUI 610, a small window 375 opens allowing the pin type (e.g., Port_0_1) and drive type (e.g., Port_0_1_Drive) to be configured. Referring now to window 620 of Figure 5B, the pin type may include analog input or analog output or global bus, etc. Referring now to window 630 of Figure 5C, the drive type may include high-z, pull-up, pull-down, strong, etc. The windows 620 and 630 may include a list that contains items that can be selected using the cursor. When the cursor is clicked outside of the windows 620 or 630, then the windows 620, 630 disappear automatically.

Please replace the paragraph beginning at page 17, line 17 with the following new paragraph:

Pin configuration is described in co-pending U.S. patent application serial number 10/032,986, filed October 29, 2001, entitled "PIN-OUT CONNECTIONS/DRIVE LEVELS DIRECT-SET BY DROP DOWN LIST," by Ogami et al., attorney docket number CYPR-CD01173M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 17, line 23 with the following new paragraph:

Referring now to Figure 6A-6D and to step 280 of Figure 2, the user selects programmable system block 410 interconnectivity. Embodiments provide many different windows to assist the user in setting various parameters to specify interconnectivity of programmable system blocks 410.

Referring to Figure 6A, the user may cause window 605 to appear to configure the analog output buffer. Referring to Figure 6B, the user may cause a clock window 606 to appear by clicking on a clock MUX 616 to configure which clock will be the input to a column of analog programmable system blocks 410b. Referring to Figure 6C a port selection window 607 is shown. The port selection window 607 may be made to appear by clicking on or near the pin input MUX 608. The user may then select the input port. Referring now to Figure 6D, the user may click on or near the analog clocking MUX 614 to cause a window 613 to appear to select which digital programmable system block 410a should be selected by the clock MUX (616 of Figure 6B).

IN THE CLAIMS

Please amend the claims as follows:

8. (AMENDED) The method of Claim 1, wherein said graphical user interface represents a plurality of digital and analog programmable system blocks, wherein said module maps to at least one of said blocks.

IN THE ABSTRACT

Please replace the Abstract with the following new Abstract:

A method to program a microcontroller using a software program. First a user selects a module from a catalog of available modules. The module may be for implementing an amplifier, timer, pulse width modulator, etc. This causes information related to the selected module to be displayed. For example, a schematic and data sheet for the selected module may be displayed. Next, the user requests a position and places the selected module in a graphical user interface, which represents the resources available to implement the available modules. For example, the resources may be programmable system blocks. Additional user modules may then be selected and placed. The user then configures the circuit by selecting circuit parameters for the user modules (e.g.,

amplifier gain), pin configurations, and interconnections between programmable system blocks. The user may then edit source code used to cause the user modules to perform their functions.

AMENDMENTS WITH CHANGES SHOWN:

IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 4 with the following new paragraph:

The present invention relates to the field of programmable single-chip systems [on a chip (PSoCs)]. Specifically, the present invention relates to a method for designing a circuit to be implemented in a target device, such as a microcontroller, using a graphical software program.

Please replace the paragraph beginning at page 4, line 10 with the following new paragraph:

A method to facilitate circuit design using a software program with a graphical user interface is disclosed. First a user selects a module from a catalog of available modules. The module may be for implementing an amplifier, timer, pulse width modulator, etc. This causes information related to the selected module to be displayed. For example, a schematic and data sheet for the selected module may be displayed. Next, the user requests a position and places the selected module in a graphical user interface, which represents the resources available to implement the available modules. For example, the resources may be programmable system [on a chip (PSoC)] blocks. Additional user modules may then be selected and placed.

Please replace the paragraph beginning at page 4, line 21 with the following new paragraph:

The user then configures the circuit by selecting circuit parameters for the user modules (e.g., amplifier gain), pin configurations, and interconnections between [PSoC] programmable system

blocks. The user may then edit source code used to cause the user modules to perform their functions.

Please replace the paragraph beginning at page 5, line 1 with the following new paragraph:

Another embodiment allows the user to select a new position (e.g., new [PSoC] programmable system block or blocks) for a selected user module. In response to such a user request, a new potential position is computed and displayed for the user module.

Please replace the paragraph beginning at page 7, line 6 with the following new paragraph:

Figure 6A, Figure 6B, Figure 6C, and Figure 6D are illustrations of graphical user interfaces for configuring interconnections between [PSoC] programmable system blocks, according to an embodiment of the present invention.

Please replace the paragraph beginning at page 9, line 2 with the following new paragraph:

Referring now to Figure 1B, a user module placement work-space includes a resource graphic window 360 illustrating the placement of user modules 304 with respect to the available resources (e.g., available [PSoC] programmable system blocks 410 of a microcontroller) in a hardware layout graphical display. Throughout this application the term resource image may denote the blocks 410 upon which user modules 304 are placed in window 360. As the resource images may represent [PSoC] programmable system blocks in one embodiment, the resource images may be referred to as [PSoC] programmable system blocks for convenience. It will be understood that the resource images may represent other resources however, as the present invention is not limited to implementing the user modules 304 in [PSoC] programmable system blocks. Figure 1B shows a number of digital [PSoC] programmable system blocks 410a along the top row (e.g., the blocks labeled DBA00, DBA01, etc.), as well as four columns of analog [PSoC] programmable system

blocks 410b (e.g., the blocks labeled ACA00, ACA01, etc.). The present invention is well suited to using any number of analog and digital [PSoC] programmable system blocks 410. Furthermore, the blocks in graphic window 360 are not limited to representing [PSoC] programmable system blocks.

Please replace the paragraph beginning at page 9, line 19 with the following new paragraph:

A single user module 304 may map to one or more [PSoC] programmable system blocks 410. Color coding (not shown) may be used to relate the user modules 304 of selected modules window 306 with their schematic placement in resource graphic window 360. The analog 410b and digital 410a [PSoC] programmable system blocks may be more generally defined as two different classes to which a user module 304 maps. The present invention is well-suited to having many different classes.

Please replace the paragraph beginning at page 10, line 2 with the following new paragraph:

Referring now to Figure 1C, a pin-out configuration work-space is shown. The pin-out configuration work-space allows the user to connect [PSoC] programmable system blocks 410 to input/output (I/O) pins, as well as configure the I/O pins' drive characteristics. In one embodiment, a pin configuration window 380 may be used to configure pins. Pin configuration window 380 has a port column 381, a select column 382, and a drive column 383. In another embodiment, a user may [to] set pin configurations by clicking on the GUI of the chip 610. The operation of these features will be discussed more fully herein.

Please replace the paragraph beginning at page 11, line 11 with the following new paragraph:

User modules 304 may require multiple [PSoC] programmable system blocks 410 to be implemented. In some cases, user modules 304 may require special ports or hardware which will

limit the number of [PSoC] programmable system blocks 410 that can be used for their implementation. The process of mapping a user module 304 to [PSoC] programmable system blocks 410, such that the user module 304 is realized within the microcontroller, may be referred to as "user module placement." An embodiment automatically determines the possible placements of a user module 304 based on an Extensible Markup Language (XML) user module description and the hardware description of the underlying chip. However, the present invention is not limited to using XML descriptions. The potential placement positions may be automatically inferred based on the XML input data. Therefore, the placement process of embodiments of the present invention is data driven.

Please replace the paragraph beginning at page 11, line 24 with the following new paragraph:

Referring to step 220 of Figure 2, a user then requests a possible placement for a user module 304 in the resource area 360. One or more [PSoC] programmable system blocks 410 may be highlighted to indicate a possible position for the user module 304 based on, for example, XML input data. For example, referring to Figure 1B, the ADCINC12_1 user module 304 has been selected for placement in the window 360. This user module 304 requires two digital blocks 410a and one analog block 410b. The digital [PSoC] programmable system blocks 410a labeled DBA00 and DBA01 are highlighted to indicate a possible position for the ADCINC12_1 user module 304. Referring now to Figure 3A, the analog [PSoC] programmable system block [410a] 410b labeled ASB20 is highlighted to indicate that it is a possible position for the analog portion of the ADCINC12_1 user module 304. Embodiments may use color coding to associate the highlighting color with a unique color assigned to that user module 304.

Please replace the paragraph beginning at page 12, line 12 with the following new paragraph:

User module placement is described in co-pending U.S. patent application serial number [ ] 09/989,762, filed concurrently herewith, entitled "A SYSTEM AND METHOD FOR PERFORMING NEXT PLACEMENTS AND PRUNING OF DISALLOWED PLACEMENTS FOR PROGRAMMING AN INTEGRATED CIRCUIT," by Ogami et al., attorney docket number CYPR-CD01175M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 12, line 19 with the following new paragraph:

Referring now to Figures 3A-3C and to step 240 of Figure 2, after placing a user module 304, a user may desire to move it to another [PSoC] programmable system block 410 (or blocks). In step 240, the user may request a new position for the user module 304 by, for example, clicking a next placement icon 371. In response to this, a new placement may be computed and displayed. Figures 3A-3C illustrate three possible positions for the analog portion of the ADCINC12_1 user module 304. Placements that are incompatible with the user module requirements are automatically pruned out by the software and therefore are not displayed as valid placements. In one embodiment, all positions are shown to the user, sequentially, each time the next placement icon 371 is selected. However, if a potential placement involves a [PSoC] programmable system block 410 that has already been used (e.g., by another placed user module 304), then in these cases the place user module [372] icon 372 is grayed out indicating that this placement is only valid if the resources were vacant. This allows the user to see all possible placements.

Please replace the paragraph beginning at page 14, line 1 with the following new paragraph:

Referring now to step 250 of Figure 2, the user may then select the new position by clicking on the select position button 372 when the user module 304 is on the desired [PSoC] programmable system block or blocks 410.

Please replace the paragraph beginning at page 14, line 5 with the following new paragraph:

User module next placement is described in co-pending US patent application serial number [ ] 09/989,781, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR DECOUPLING AND ITERATING RESOURCES ASSOCIATED WITH A MODULE," by Ogami et al., attorney docket number CYPR-CD01180M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 14, line 12 with the following new paragraph:

The user may repeat steps 210 through 250 to add more user modules 304. Each time a new user module is selected, a system resource window is updated. Referring again to Figure 1A, for each User Module 304 selected, the system updates the data in a resource manager window 350 with the number of occupied [PSoC] programmable system blocks 410, along with RAM and ROM usage used by the current set of "selected" User Modules 304. The system may also prevent a user from selecting a User Module 304 if it requires more resources than are currently available. Tracking the available space and memory of configurations for the design may be performed intermittently during the whole process of configuring the microcontroller. There is also a live graph tracking the [PSoC] programmable system blocks 410 used by percentage. The RAM and ROM monitors track the amount of RAM and ROM required to employ each selected User Module 304.

Please replace the paragraph beginning at page 15, line 1 with the following new paragraph:

After the user has selected one or more user modules 304, the user selects global parameters and user module parameters. Embodiments allow a user to select user module parameters, such as, for example, the gain of an amplifier, a clock speed, etc. Referring now to Figure 4 and to step 260 of Figure 2, in response to a user clicking on a region on a [PSoC] programmable system block 410 an interface 510 is displayed which allows the setting of user module parameters. For example, the

user may place "the cursor" over the lower-left corner of a [PSoC] programmable system block 410 to set input parameters. The system may display a superficial chip or a changed cursor in response to this. The user may then left-click a mouse, for example, to bring up a user module parameter window 510 to configure the user module input parameters. The process may be repeated in the lower-right corner of the [PSoC] programmable system block 410 for output parameters and on the upper-left corner for clock parameters. The present invention is not limited to these steps for bringing up a user module pop-up window 510, however. The system may then display the selected parameters in a user module parameter window 520. Various pop-up windows may be data driven in that the contents of the pop-up window may depend on, for example, the user module 304 selected. Alternatively, user parameters may be set in the user module parameter window 520.

Please replace the paragraph beginning at page 15, line 20 with the following new paragraph:

When the user module 304 is placed (e.g., instantiated) on a particular [PSoC] programmable system block 410 the register settings and parameter settings are mapped to a physical register address on the chip. This also associates interrupt vectors that the user module 304 uses based on the [PSoC] programmable system block 410. Each of the digital blocks 410a maps to one vector and each column of analog blocks 410b maps to another vector. Once the user modules 304 are placed and the parameters are set, all the physical address registers that are associated with that user module 304 are fixed and the register values are determined.

Please replace the paragraph beginning at page 16, line 12 with the following new paragraph:

Referring now to Figures 5A-5C and to step 270 of Figure 2, the user selects input/output pin configurations. One embodiment provides for a graphical user interface for facilitating the configuration of I/O pins in a microcontroller software design tool. By specifying a [PSoC] programmable system block 410 to a pin-out, a user may make a physical connection between the

software configuration and the hardware (e.g., the microcontroller). Each pin has a pin number associated therewith. Referring to Figure 5A, when the user clicks on a pin of GUI 610, a small window 375 opens allowing the pin type (e.g., Port_0_1) and drive type (e.g., Port_0_1_Drive) to be configured. Referring now to window 620 of Figure 5B, the pin type may include analog input or analog output or global bus, etc. Referring now to window 630 of Figure 5C, the drive type may include high-z, pull-up, pull-down, strong, etc. The windows 620 and 630 may include a list that contains items that can be selected using the cursor. When the cursor is clicked outside of the windows 620 or 630, then the windows 620, 630 disappear automatically.

Please replace the paragraph beginning at page 17, line 17 with the following new paragraph:

Pin configuration is described in co-pending U.S. patent application serial number [_____] 10/032,986, filed October 29, 2001, entitled "PIN-OUT CONNECTIONS/DRIVE LEVELS DIRECT-SET BY DROP DOWN LIST," by Ogami et al., attorney docket number CYPR-CD01173M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 17, line 23 with the following new paragraph:

Referring now to Figure 6A-6D and to step 280 of Figure 2, the user selects [PSoC] programmable system block 410 interconnectivity. Embodiments provide many different windows to assist the user in setting various parameters to specify interconnectivity of [PSoC] programmable system blocks 410. Referring to Figure 6A, the user may cause window 605 to appear to configure the analog output buffer. Referring to Figure 6B, the user may cause a clock window 606 to appear by clicking on a clock MUX 616 to configure which clock will be the input to a column of analog [PSoC] programmable system blocks 410b. Referring to Figure 6C a port selection window 607 is shown. The port selection window 607 may be made to appear by clicking on or near the pin input

MUX 608. The user may then select the input port. Referring now to Figure 6D, the user may click on or near the analog clocking MUX 614 to cause a window 613 to appear to select which digital [PSoC] programmable system block 410a should be selected by the clock MUX (616 of Figure 6B).

IN THE CLAIMS

Please amend the claims as follows:

8. (AMENDED) The method of Claim 1, wherein said graphical user interface represents a plurality of digital and analog programmable system [on a chip (PSoC)] blocks, wherein said module maps to at least one of said [PSoC] blocks.

IN THE ABSTRACT

Please replace the Abstract with the following new Abstract:

A method to program a microcontroller using a software program. First a user selects a module from a catalog of available modules. The module may be for implementing an amplifier, timer, pulse width modulator, etc. This causes information related to the selected module to be displayed. For example, a schematic and data sheet for the selected module may be displayed. Next, the user requests a position and places the selected module in a graphical user interface, which represents the resources available to implement the available modules. For example, the resources may be programmable system [on a chip (PSoC)] blocks. Additional user modules may then be selected and placed. The user then configures the circuit by selecting circuit parameters for the user modules (e.g., amplifier gain), pin configurations, and interconnections between [PSoC] programmable system blocks. The user may then edit source code used to cause the user modules to perform their functions.

SUPPORT FOR AMENDMENTS

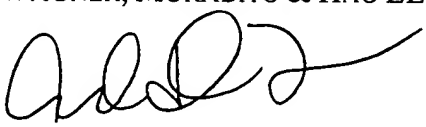
Support for the amendments herein can be found throughout the specification (e.g., page 4, lines 10-19), Title and Abstract as originally filed, and in the copending applications cited in the specification. The present amendment intends to remove references to the trademarks of Cypress MicroSystems, Inc. (see, e.g., M.P.E.P. § 608.01(v) and the attached printouts from http://tess.uspto.gov/, notably the "PSOC" trademark registration information therein, and http://www.cypressmicro.com/corporate/CY_Announces_nov_13_2000.html). No new matter is introduced.

REMARKS

Claims 1-20 are presented for consideration in the present application, which is now believed to be in condition for examination. Early notice to that effect is earnestly solicited.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP



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Typed Drawing

Word Mark	PSOC
Goods and Services	IC 009. US 021 023 026 036 038. G & S: semiconductors devices; microprocessors; and integrated microelectronic devices in the nature of semiconductors devices
Mark Drawing Code	(1) TYPED DRAWING
Serial Number	75951037
Filing Date	March 3, 2000
Filed ITU	FILED AS ITU
Published for Opposition	November 12, 2002
Owner	(APPLICANT) Cypress MicroSystems, Inc. CORPORATION DELAWARE 12230 N. E. Woodinville Drive Suite A Woodinville WASHINGTON 98072
Attorney of Record	John Weber
Type of Mark	TRADEMARK
Register	PRINCIPAL
Live/Dead Indicator	LIVE

CYPRESS MICROSYSTEMS UNVEILS PROGRAMMABLE SYSTEM-ON-A-CHIP FOR EMBEDDED INTERNET, COMMUNICATIONS AND CONSUMER SYSTEMS

PSoC™ Devices Integrate Programmable Analog and Digital Functions To Simplify Design Of Wireless, Handheld, Data Communications, and Industrial Systems

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WOODINVILLE, Wash., November 13, 2000 - Cypress MicroSystems, a subsidiary of Cypress Semiconductor, today introduced a family of programmable system-on-a-chip (PSoC™) devices, designed to implement a single, configurable device on MCU-based system boards. As general purpose solutions, PSoC devices are targeted for implementation in embedded applications, including audio, wireless, handheld, data communications, Internet control, industrial, and consumer systems.

PSoC devices integrate a fast microcontroller, SONOS™-based (Silicon Oxide Nitride Oxide Silicon) Flash memory and SRAM, and programmable arrays of analog and digital system functions - known as PSoC blocks - in low-cost, small-footprint packages. To save designers time, Cypress Microsystems also offers User Modules - pre-designed peripherals comprised of PSoC blocks. By selecting a PSoC with the needed resource combination of memory, PSoC blocks and pins, designers have a device that reduces costs by eliminating external chips and simplifying system design.

"Today there are thousands of different 8-bit microcontrollers on the market, and designers still have trouble finding one that is a perfect fit for their application. In addition, embedded applications require analog peripherals that usually call for additional external devices," said Mike Polen, Cypress MicroSystems's vice president of marketing. "Engineers know that the perfect solution is a custom-designed system-on-a-chip, but custom microcontrollers, ASICs and PLDs are expensive, require very large volumes or call for specialized design skills."

"In contrast, the Cypress Microsystems PSoC solution offers custom configurations, takes no time or special expertise to create, incurs no NRE, and integrates both analog and digital functions," continued Polen. "These factors make the cost of the PSoC solution competitive with standard microcontrollers."

SONOS - a proprietary Cypress process technology - is key to Cypress Microsystems's system-on-a-chip. SONOS is a cost-effective, electrically-erasable, programmable, non-volatile memory structure that speeds time-to-market at a cost that is comparable with commodity devices. SONOS is also being implemented in Cypress Semiconductor's frequency timing generators, USB controllers and intelligent control network devices.

About PSoC blocks and User Modules

After a review of the peripherals found in microcontrollers and the analog ICs used in typical designs, Cypress Microsystems engineers selected a variety of digital and analog peripherals, then created PSoC blocks, or system-on-a-chip blocks, and integrated them into each PSoC device. Users select the functions they need and configure the PSoC blocks on the PSoC device accordingly.

Digital PSoC blocks are 8-bit peripherals that can be programmed to perform a variety of functions by changing the contents of a few registers. They can be configured as timers, controllers, serial communications ports, CRC generators, or pseudo-random number generators. They can be connected in series to handle more complex functions - for example, a 24-bit timer is three connected 8-bit PSoC blocks acting as timers.

Analog PSoC blocks consist of programmable operational amplifier circuits that can be configured to perform a set of typical analog peripheral functions. Analog PSoC blocks can be programmed by setting a few registers to interconnect and trim the appropriate operational amplifier circuit to create the desired result. Among the typical peripherals that can be created are amplifiers, DACs, ADCs, analog drivers, and high-, low- and band-pass filters.

To eliminate the need for customers to understand PSoC blocks in-depth and further shorten development time, Cypress Microsystems developed User Modules, preconfigured peripherals created from PSoC blocks. User Modules allow customers to select the functions they need and automatically integrate the necessary PSoC

blocks into their PSoC device.

Software Support

Cypress Microsystems will offer PSoC Designer™, a complete development system to support the PSoC device. The system will include a C compiler and assembler, a linking and debugging tool, an in-circuit emulator, and the Device Editor™.

Designers can use the Device Editor and its graphical interface to configure a PSoC device by dragging the desired peripherals or functions - from a library of User Modules - into the part. The selected User Modules are then automatically mapped onto the available PSoC blocks.

On-chip Flash program memory stores each PSoC device's parameters, allowing the user to reprogram the device during production, during system test or in the field. PSoC devices may even be self-reprogrammed remotely.

"PSoC devices are like a screwdriver with replaceable bits," stated Nathan John, Cypress Microsystems's director of marketing. "They can be configured and reconfigured as the design progresses and functional requirements change. They provide a core set of analog and digital functions that eliminate the need for additional devices. And they can be programmed to custom-fit any application."

Availability and Pricing

Cypress Microsystems will initially offer the following PSoC devices:

Part Number	Max. Speed	Package	Samples	Production	Price (Q 1,000)
CY8C25122	24 MHz	8-pin DIP	Q1 2001	Q1 2001	$ 1.76
CY8C26233	24 MHz	20-pin DIP 20-pin SOIC 20-pin SSOP	Q1 2001	Q1 2001	$ 2.21
CY8C26443	24 MHz	28-pin DIP 28-pin SOIC 28-pin SSOP	Q4 2000	Q1 2001	$ 2.79
CY8C26643	24 MHz	48-pin DIP 48-pin SSOP 48-pin TQFP	Q1 2001	Q1 2001	$ 3.53

About Cypress Microsystems

Cypress Microsystems designs, develops, manufactures and markets high-performance, field programmable integrated micro-based solutions for high-volume embedded control functions in computer, communications, consumer and control applications. Established as a subsidiary of Cypress Semiconductor Corporation in the fourth quarter of 1999, Cypress Microsystems's stockholders are its employees and Cypress Semiconductor. The close association with Cypress Semiconductor allows access to their process and design technology, and field sales and applications forces. Cypress Microsystems is based near Seattle in Woodinville, Washington.

The Cypress Microsystems PsoC™ family of programmable system-on-a-chip devices will replace many MCU-based system boards with one single-chip, programmable PSoC. A single PSoC device provides a fast microcontroller, SONOS™ FLASH and SRAM memory, and configurable analog and digital peripheral blocks in a range of convenient pin outs and memory sizes. This new product family will bring the cost and time-to-market advantages of programmable technologies, such as CPLDs and FPGAs, to the emerging system-on-a-chip marketplace.

More information about Cypress Microsystems and its products can be accessed through its Web site at www.cypressmicro.com.

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Statements in this press release regarding Cypress Semiconductor's business that are not historical facts are "forward-looking statements" involving risks and uncertainties, including but not limited to: the effect of global economic conditions, shifts in supply and demand, market acceptance, the impact of competitive products and pricing, product development, commercialization and technological difficulties, and capacity and supply constraints. Please refer to Cypress Semiconductor's Securities and Exchange Commission filings for a discussion of such risks.

CYPR-CD01168M

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

Manfred BARTZ et al. : GROUP ART UNIT:

SERIAL NO: 09/989,571 :

FILED: NOVEMBER 19, 2001 : EXAMINER:

FOR: METHOD FOR DESIGNING A CIRCUIT FOR PROGRAMMABLE MICROCONTROLLERS

REQUEST FOR APPROVAL OF DRAWING CHANGES

COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant respectfully requests approval of the drawing changes shown in the attached sheet. The changes are intended to remove references to the trademarks of Cypress MicroSystems, Inc. (e.g., "PSoC"). No new matter is introduced.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

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Andrew D. Fortney, Ph.D.
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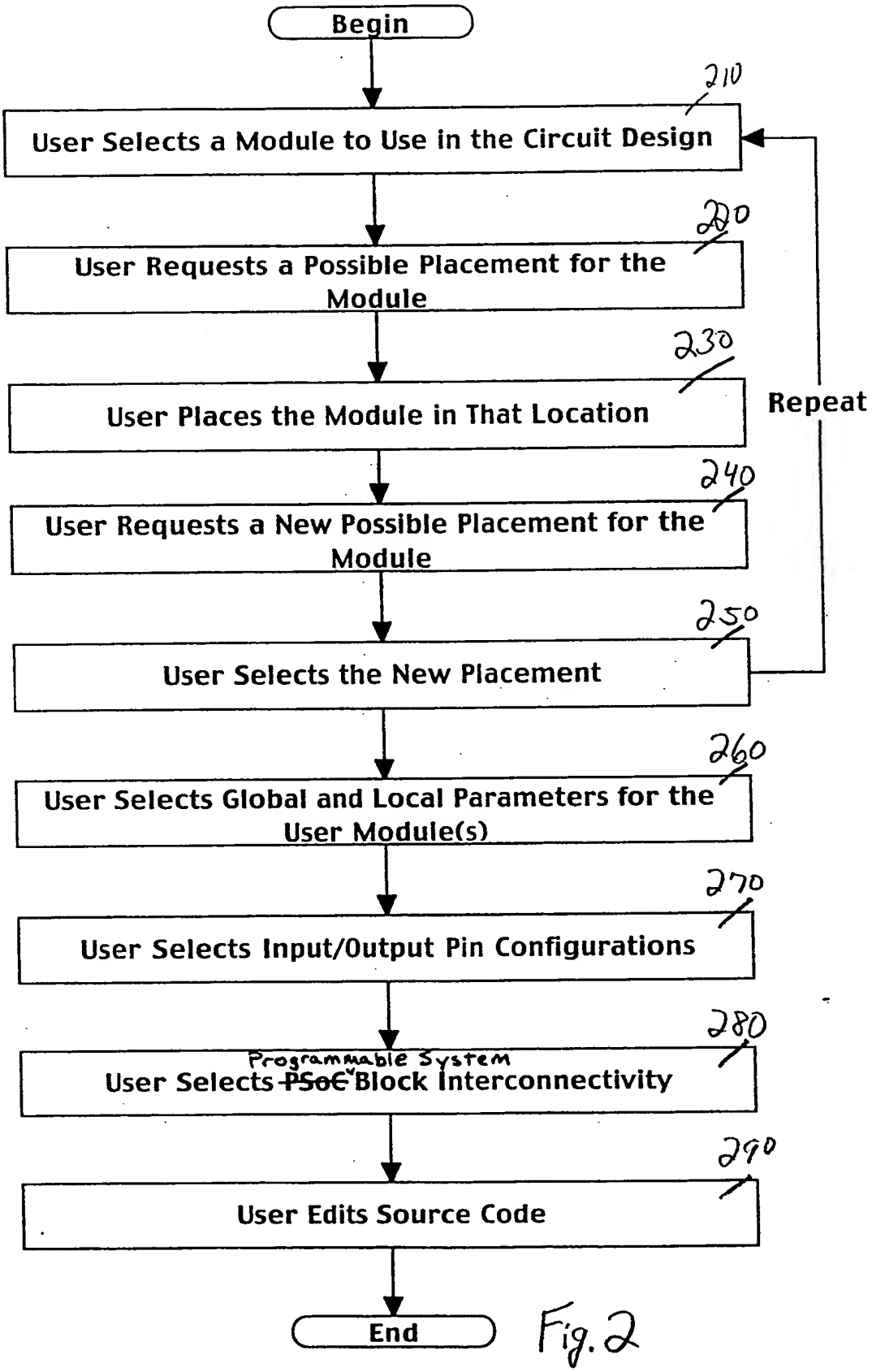
Begin
210
User Selects a Module to Use in the Circuit Design
220
User Requests a Possible Placement for the Module
230
User Places the Module in That Location
Repeat
240
User Requests a New Possible Placement for the Module
250
User Selects the New Placement
260
User Selects Global and Local Parameters for the User Module(s)
270
User Selects Input/Output Pin Configurations
280
User Selects ~~PSoC~~ Programmable System Block Interconnectivity
290
User Edits Source Code
End

Fig. 2

Attorney Docket No.: YPR-CD01168M

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the U.S. Patent and Trademark Office, Washington, D.C., 20231, on the below date of deposit.					
Date of Deposit:	01/27/03	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

In re Application of: Manfred Bartz, Marat Zhaksilikov, Steve Roe, Kenneth Y. Ogami, Matthew A. Pleis and Douglas H. Anderson

Serial No.: 09/989,571

Examiner: not yet assigned

Filed: 11/19/01

Art Unit: 2673

For: METHOD FOR DESIGNING A CIRCUIT FOR PROGRAMMABLE MICROCONTROLLER

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

X Transmitted herewith is a response to an office action for the above identified patent application. (19 sheets)
X Transmitted herewith are 1 sheets of Red Line drawings.
X Drawing Amendment 1 sheet
X Supporting Documents 4 sheets

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [ ] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[ ] one month	$110.00
[ ] two months	$410.00
[ ] three months	$930.00
[ ] four months	$1,450.00

Fee $ _____

If an additional extension of time is required, please consider this a petition therefor.

(b) [X] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	20	- 20 =	0	x $18.00	$0.00
Independent Claims	3	- 3 =	0	x $84.00	$0.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$260.00	$0.00
Total Fees					$0.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
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San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date:_____

By:_____
Anthony C. Murabito
Reg. No. 35,295